## COMPUTER AIDED ANALYSIS OF DIGITAL COMPONENTS IN PRODUCTION PROCESS

## Aleksandr KATKOW

**Abstrakt**: The process of production contemporary digital devices is a complex computer aided process. The process of production of modern digital devices are highly dependent on the quality of digital components, and especially from their temporal characteristics. In this article the methods of determining the time parameters of digital devices on the basis of the time parameters of components are examined. The possibility of the methods of continuous logic with the analysis of transient processes in the digital units is examined. It shows that it is expedient to use the technical parameters of digital components obtained in the process of their production with the analysis of the time parameters of digital units.

Key words: Computer aided production, Digital device parameter, Transient processes.

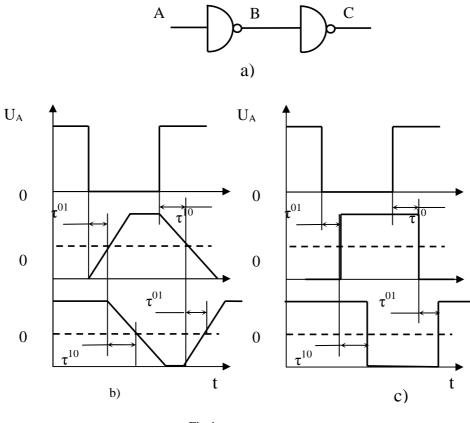
During the construction of digital units the calculation of real physical parameters of elements has great significance[1]. Especially it is important with the development of the digital modules, in which there is no general synchronization for the environment and digital automaton, and the environment, which functions in the general case in the continuous time, acts on the entrances of automaton and it thus initiates its working. It is completely clear that since the real logic elements receive at the entrances and generate at the outputs signals it is limited by spectrum, signals with the infinitely steep leading edge and steep trailing edge in the real digital circuits are not encountered. Being the filter of low frequency, logic element during the supplying to it to the entrance of signal with the infinite steepness edge at the output forms signal with the sloping leading edges.

Let us suppose to the circuit of two inverters (Fig. 1, a) is given signal "log. 0" with the ideally rectangular edges (Fig. 1, b, c). Because of the filtering properties of logic element at its output we will obtain the signal, leading edge and trailing edge in which with practical accuracy they frequently approximate by the straight lines (Fig. 1, b). In this case, taking into account the threshold properties of logic element, set that the signal at the output is equal "log. 1", if voltage on the input higher than value of threshold level  $U_T$ , and is equal "log. 0", if it lower than  $U_T$ .

Delay time to the switch on  $\tau_{01}$  of logic element is counted off from the moment, when input signal reached threshold level, to the moment, when output signal reaches threshold level. Analogously is determined delay time to the switch off  $\tau_{10}$ . The signal with the same delays for the switch on and the switch off is formed at the output of the second logic element in the circuit. Frequently occurs the inequality of  $\tau_{01} \neq \tau_{10}$ . Their relationship takes in account by different slope of the inclination of straight lines upon transfer from the state "log. 1" into "log. 0" and vice versa. For the analysis of transient processes in the logic circuits it is convenient to use an apparatus of continuous or infinitely-valued logic [2]. However, let us note that the introduction of the value of threshold divides off entire range of values of the output voltage of logic element on two parts.

One part of them with  $U_{out} > U_T$  is received by the following logic element as signal "log. 1", and the second part of them with  $U_{uot} < U_T$  as signal "log. 0". This circumstance

makes it possible to consider signals at the entrances and the outputs as square-wave, but moved relative to each other the delay time to the switch on and switch off respectively (Fig. 1, c). This representing of signals gives the same result as approximation by their inclined straight lines. We analyze transient process in the conjunctor (Fig. 2, a) with the appearance at its entrances of two signals  $A_1$  and  $A_2$  moved relatively on the interval of the time  $\Theta$ , from which  $A_1$  is changed from "log. 1" to "log. 0" and  $A_2$  is changed from "log. 0" to "log. 1" (Fig. 2, b, c). Through the time interval, equal  $\tau^{01}$ , from the moment, when the input signal  $A_2$  exceeds threshold level and will be interpreted by conjunctor as "log. 1", at the output of conjunctor signal will reach threshold level and will be during exceeding of it classified as "log. 1" (Fig. 2, b).





However, after time  $\Theta$  signal A<sub>1</sub> becomes below threshold level and is interpreted by the entrance of conjunctor as "log. 0». From this point of time is formed the process of the switching off by conjunctor. When the output signal of conjunctor becomes below threshold level, thus is classified as "log. 0». The shaded region of correspondent to the interval of the time, when at the output of conjunctor is a signal "log. 1". In the hypothetical model with the signals with the infinitely steep leading edge and steep trailing edge and two parameters - the intervals of delay time to the switching on  $\tau^{01}$  and intervals of delay time to the switching on process flows as follows: through  $\tau^{01}$  from the moment of establishing the

signal A<sub>2</sub> (Fig. 2, c) in "log. 1" at the output of conjunctor will appear signal "log. 1", which after a change of the signal A<sub>1</sub> in "log. 0" also with delay time  $\tau^{10}$  converts to state "log. 0".

Let us build transient process in the conjunctor taking into account the possible dispersion of time of delays. In Fig. 2,d,e are shown the output signals of conjunctor, built on the assumption that of the delay of  $\tau^{01}$  and  $\tau^{10}$  are increased in comparison with the previous case by 60%. In this case signal "log. 1" at the output of conjunctor not at all take place. Analogous results are obtained by other authors ,who show that the signals at the output of logic element do not appear, if the duration of input signals does not exceed delay time for the switch on and switch off respectively. We will consider that if the duration of signal on the entrance of logic element is within the limits of  $\tau^{01} < \Theta < 2\tau^{01}$  upon transfer from "log. 1" or in the limits of  $\tau^{10} < \Theta < 2\tau^{10}$  upon transfer from "log. 1" to "log. 0".

With these conditions the duration of output signal is defined according to the formulas

$$t^{01} = (\Theta - \tau^{01})(1 + \tau^{10}/\tau^{01})$$
(1)  
$$t^{10} = (\Theta - \tau^{10})(1 + \tau^{01}/\tau^{10}),$$

with the level of threshold  $U_T = 0.5U_1$ . In practice, the threshold properties of digital components are significant changes, depending on the quality of the process of production. This parameter is very difficult to control and therefore more frequently in the analysis of the temporal characteristics of the components taken threshold is close to half the voltage signal corresponding to the logical unit. This same assumption was adopted in the analysis of transients on the temporal characteristics of the process of switching logic element of the state of the logical unit in the state of logical zero. It is assumed that the switching time from the state of the logical unit in the state of logical zero are equal.

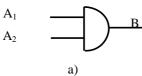
These formulas are used with the condition that the process of switch on and switch off of the logic element starting immediately upon transfer of the input signal through the threshold level. The durations of delays for the process of switch on and switch off linearly depending on how up to the moment of this transition output signal is differed from threshold level, not achieving of value "log. 0" or "log. 1". Formulas (1) is simplified with the condition of  $\tau^{01} = \tau^{10}$ :

$$t^{01} = 2(\Theta - \tau^{01}) t^{10} = 2(\Theta - \tau^{10})$$

As we see, the results of the analysis of the transient process of conjunctor with the approximation of input and output signals by inclined straight lines after the classification of the output voltage of conjunctor according to the sign "log. 0" and "log. 1" with respect to the level of threshold coincide with the results, obtained on the model, which operates only with two parameters - delays to switch on and switch off.

Subsequently we will not consider the nature of a change of the signals in the subthreshold and after-threshold zones at the entrances and the outputs of logic elements, since diagnostics of the behavior of logic circuits on the development of transient process after threshold level below be examined will not be. Thus, noting that the signals in the real diagram never can have infinitely steep edges and what their simplest and convenient approximation is, apparently, linear, we will operate only with the signals, which in the case of equality or threshold crossing level are interpreted as signals "log. 1", and into the cases - "log. 0". For simplicity of conducting studies of transient processes in the logic circuits let us agree to operate with the analysis only with times of their delays to the switch on and switch off  $(\tau^{01}, \tau^{10})$ , taking into account inertia properties of logic elements connected with these parameters. We will in other words, assume that:

- 1) logic elements operate with square-wave signals;
- a change of the parameters of the functioning of logic element in the dependence on the capacity of load C<sub>out</sub>, temperature T, value of the threshold level U<sub>T</sub> and fluctuations of the feeding voltage E affects only a change in the time of delays for the switch on and the switch off τ<sup>01</sup> = τ<sup>01</sup>(C<sub>out</sub>, T, U<sub>T</sub>, E), τ<sup>10</sup> = τ<sup>10</sup>(C<sub>out</sub>, T, U<sub>T</sub>, E);
  the inertia properties of logic elements about appear in the fact that signal "log. 0" or
- 3) the inertia properties of logic elements about appear in the fact that signal "log. 0" or "log. 1" at their outputs take place only in the case, when the duration of signal at the entrance is not lower than the delay of  $\tau^{01}$  and  $\tau^{10}$  respectively;
- 4) delays in the circuits, which connect the logic elements between themselves, are equal to zero, it means that the circuits of communications are inertia-free.



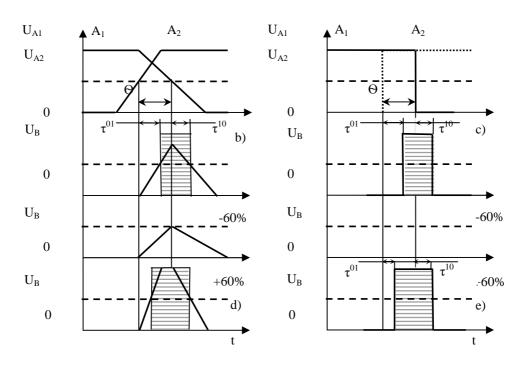


Fig. 2

The limitations indicated lead us to the equivalent circuit of logic element. In it logic element is considered ideal, and its output signals at any moment of time are equal to Boolean function of input signals. The inertia properties of logic element are considered by inertia parasitic delay  $\tau$  (1,0) [3], which changes depending on whether works this element on the switch on or the switch, moreover  $\tau$  (1) =  $\tau^{01}$  and  $\tau$  (0) =  $\tau^{10}$ .

Thus, the duration of transient process in the logic element, strictly speaking, depends on state, into which it comes over, since  $\tau(1) \neq \tau(0)$ , but this circumstance is not always considered, they frequently consider for simplicity that  $\tau(1) = \tau(0) = \tau_i = \tau$ . Such more simple the model is necessary when task it consists of the checking, can occur the undesirable behavior of circuit. If it appears with the adopted assumptions, then it can arise, also, in the real circuit, in which all variations in the delay factors are in the first approximation, equally probable and, consequently, also simplified model it can prove to be sufficiently precise.

At present the creation of quick special operating digital systems (industrial robots, onboard navigation complexes, controllers for automation of the physical experiments and so on) is developed in two basic directions. They are based on asynchronous principals of the organization of computational processes.

The first direction is connected with the introduction to asynchronism on about the programmed or micro programmed level of organization the calculation process. The second - with the asynchronous organization the calculation process at the circuit technology level.

In the computing systems in the majority of the cases is organized the synchronous working of the flow of data on the base of standard synchronous algorithms, microprogrammed realized in the microprocessor-based systems. Clock frequency in this case is determined by time parameters of components and by quantity of levels of the logic in the combination circuits, according to which input signals are propagated to the outputs. It is natural that the maximum clock frequency is determined by the duration of transient processes which they occur in the combination circuits. Its duration is determined by a maximum quantity of levels of logic with propagation of input signals to the outputs, and by the time parameters of logic elements, that is determined by time of delays of logic elements for the switch on and the switch off.

In connection with the fact that computational processes in the combination circuits of synchronous blocks far from always have maximum duration, introduction to synchronization leads to the fact that the combination fragments of large synchronous blocks stay the part of the time in the expectation of sync signals. This leads to the incomplete use of a speed of the combination circuits of asynchronous blocks[4]. The first step on the road to using the asynchronous calculations it is the creation of those specialized and universal computer systems, synchronous in the apparatus performance, but asynchronous with respect to program or microprogrammed realization. As starting moment with the asynchronous program realization of the work of the data processing systems serves existence of rapid asynchronous algorithms for fulfilling the operations of multiplication, of division, taking the logarithm and others. In this case a quantity of synchronous steps of algorithm is determined by the data. With the end of the fulfillment of operation it is easy to form the signal of completion, which can be used with the chain calculations for the load of obtained data as the initial into the subsequent parallel blocks. A quantity of synchronous steps of asynchronous algorithm in the computational process becomes the value of variable, which leads to more rapid obtaining of results; however, the reserves for an increase in the speed this are not contained by, since on the circuit level

organization calculate process it remains synchronous.

## Summary

In the article the method of determining the duration of transient process in the logical nets is examined. Is produced the comparison of methods one of which it is based on the application of continuous logic and with another on the use of the technological parameters of components for determining the duration of transient process in the logic circuits. The process of computer modeling of transients using two, discussed above analysis techniques give identical results. However, it is expedient to use the second method in the process of the production of digital units in view of its simplicity.

## **Bibliography**

- 1. Łuba T., Rola i znaczenie syntezy logicznej w technice cyfrowej układów programowalnych. Elektronika, str. 15, 19, nr 7-8, 2002.
- 2. Ginzburg, S. A., Mathematical continuous logic and the representation of functions, Energia, Moscow, 1968.
- 3. Brzozowski J. A, Seger C-J.: Asynchronous Circuits, Springer Verlag, New York 1995.
- 4. Katkow A. Digital modeling automata, Naukowa Dumka, Kiev, 1990.

Prof. dr hab. inż. Aleksandr KATKOW Instytut Ekonometrii i Informatyki Wydział Zarządzania Politechniki Częstochowskiej ul. Dąbrowskiego 69, 42-200 Częstochowa tel.: +48 692755863 email: katkow@zim.pcz.pl